Design and Simulation of 1.2 mW Power Consumption Ultra-Wideband Low Noise Amplifier for Ultra-Wideband Wireless Communications

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***Abstract*— Nowadays, for the field of wireless communications, the good design of radio frequency receiver for wireless communication applications is considered one of the main targets in radio frequency research. In ultra-wideband (UWB) receivers, low noise amplifier is considered the most important building block in UWB receiver structure. In this paper we provide the design and simulation of ultra-wideband low noise amplifier to get radio receiver with good performance in wireless communication application.**

This paper introduces the design and simulation of ultra-wideband low noise amplifier using 130 nm CMOS technology. This design uses three stages amplifier. The design provides bandwidth range from (3.9 GHz to 15 GHz) with power gain (S_{21}) of 10 dB. The output noise of the proposed amplifier is 300 uV_{rms}. The proposed LNA is designed using 1.2 V power supply, the dissipated power of the proposed amplifier is 1.2 mW. The proposed amplifier gives noise figure of 1.5 dB and input referred third order intercept point (IIP3) reached to 20 dBm.

Keywords*— Low Noise Amplifier (LNA), Noise Figure (NF), Output Noise, Power Dissipation, Radio Frequency (RF) Receiver, Ultra-Wideband (UWB)

I. INTRODUCTION

Today, applications of wireless communication are overgrowing, so we find that radio frequency receiver designers make great effort to design receivers to be suitable for wireless communication applications. There are great wireless communication applications that used low noise amplifier in its operation [1]. Low noise amplifier is considered the most important block in radio receiver, so if low noise amplifier performance parameters are designed correctly to satisfy the application targets, then the whole RF receiver will be operated very well. This make the design of low noise amplifier (LNA) is very important and hard role. As known ultra-wideband system is operating at frequencies reaching to 10.6 GHz [2]. So for all wireless standards they require different ranges of operating frequencies and require their performance parameters to be satisfied such as low noise figure, high bandwidth, good gain and low power dissipation [3]. As mentioned previously, all performance parameters of low noise amplifier must satisfy the requirements of all applications of wireless communication. So in order to verify this target of good performance parameters, future wireless radio receiver should have low noise amplifier with good performance to support all wireless communication standards.

So, great effort must be done to satisfy this target to design low noise amplifier with good performance. There are many different parameters that determine low noise amplifier performance such as noise figure (NF), bandwidth, power gain, sensitivity and LNA linearity [4]. The design of low noise amplifier is based on achieving good performance parameter according to the type of application, as some applications require wide bandwidth on account gain or require low power consumption on account noise figure and so on. So all the time each application requires parameters different from another application and the designer will design LNA performance parameters according to the requirements of the target application. There are different low noise amplifier design methods and techniques have been done to achieve these performance parameters. One of these methods uses two common source stages with different resonance frequencies to achieve low power consumption for LNA with high bandwidth [5]. Another method uses two common source and shunt feedback stages to achieve low noise amplifier with good bandwidth, low power and low noise figure [6].

Our design of the proposed ultra-wideband low noise amplifier is based on using three stages amplifier. First stage is common gate amplifier to achieve high impedance matching at the input, second stage is cascade common source amplifier to improve gain and bandwidth of LNA and third stage is common drain amplifier cascaded with diode connected transistor to improve noise performance of the proposed low noise amplifier. This technique for the proposed LNA will satisfy the target performance parameters such as low noise figure, high bandwidth, low output noise, low power consumption, high linearity and high power gain.

II. OVERVIEW OF ULTRA-WIDEBAND LOW NOISE AMPLIFIER

There are two most common receivers which used with all wireless communication standards, these receivers should be designed to satisfy the requirements of wireless communication standards.

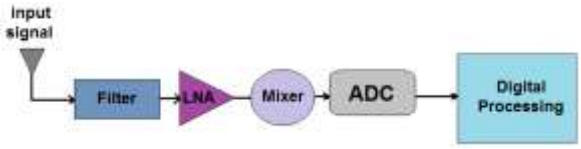

Fig. 1. Block diagram of wideband receiver (Universal receiver) [7]

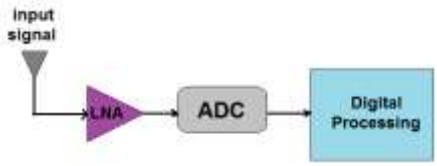

Fig. 2. Block diagram of wideband receiver (RF receiver) [7]

These receivers are universal receiver and radio frequency receiver. Universal receiver has components more than digital radio receiver in its structure. Fig. 1 shows the block diagram of the universal receiver [7]. The main universal receiver components are low noise amplifier and mixer. Mixer is used to reduce frequency conversion and this will increase the speed of analog to digital converter (ADC).

Low noise amplifier (LNA) is considered the main component or block in the receiver as it used to increase bandwidth, reduce noise and increase linearity of ADC.

The second receiver that used with radio frequency receiver is the digital radio frequency receiver. In RF receiver some component that exist in universal receiver are replaced by its digital one such as mixer and filter as shown in Fig.2. RF receiver may have main problem in its operation compared with universal one such as noise which can be introduced by RF receiver due to its sampling speed [8], [9]. So to reduce this noise, the signal to noise ratio of the input signal to RF receiver must be increased. As shown in Fig. 1 and Fig. 2, the main building block in universal receiver and RF receiver is LNA. So it is impossible to remove low noise amplifier (LNA) from the receiver. As mentioned previously, receivers that support all wireless communication standards need some performance parameters which determine its good performance such as wide-bandwidth, low noise figure, high power gain, high linearity LNA and low power dissipation. So the good design of LNA determines the good performance of RF receiver. Because of this the design of LNA with good performance parameter is still the target task for all RF receiver designers.

III. Circuitry Diagram of the Traditional and Proposed Ultra-Wideband Low Noise Amplifier

The following section provides an overview about the traditional low noise amplifier configuration. Then the proposed low noise amplifier configuration will be discussed in details. Also, a comparison between traditional and proposed LNA will be introduced and simulation results of the proposed LNA will be introduced and discussed.

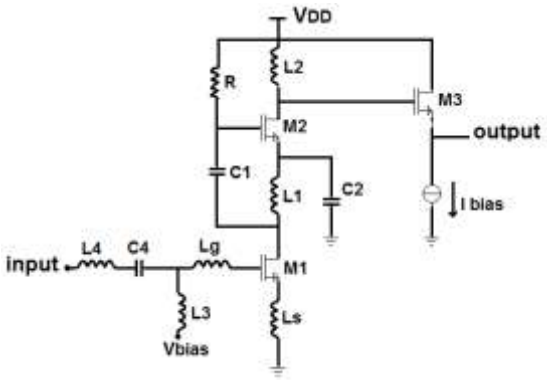

Fig. 3. Circuitry diagram of the traditional low noise amplifier [5]

A. Circuitry Diagram of the Traditional Low Noise Amplifier

Fig. 3 shows circuitry diagram of the traditional low noise amplifier. The technique which used in traditional LNA is stugger tunning technique to design one suitable for wireless communication [5]. The amplifier circuitry consists of two common source cascaded stages. Each stage will improve in performance parameter of LNA parameters. First stage is used to improve noise performance of LNA, second stage is used to improve linearity performance of LNA. Components of traditional LNA circuitry are as follow, Ls is used to provide real part of input impedance matching, Lg, L3, L4, C3 and C4 are used for increase matching at the input. M3 is the output transistor is used as buffer for output measurements. The resistor R provides bias voltage for the transistor M2. As shown in traditional LNA circuitry diagram the two stages amplifiers are stacked on each other to achieve power saving and reduce power consumption. For the coupling capacitors such as C1 and C2, C1 is used for coupling between two stages and C2 act as AC ground at source of M2. The value of these two coupling capacitors in this design is chosen to be very high to provide better coupling. The main problem in this design technique is the type of the two coupling capacitors which is Metal-Insulator-Metal (MIM) capacitors and there high values. This type of capacitor will have parasitic capacitance between bottom plate of the capacitor and the ground and this will affect the performance of LNA. Also, because the capacitors high values this will reduce the bandwidth of the LNA. In the following section the proposed LNA is introduced. The proposed LNA will solve the problem of reduction in bandwidth in traditional one, also, will solve the problem of large values of coupling capacitors and noise performance of traditional one.

B. Circuitry Diagram of the Proposed Ultra-Wideband Low Noise Amplifier

Fig. 4 shows the proposed LNA circuitry diagram. The proposed LNA amplifier circuitry has common gate (CG) as input stage with two cascaded common source stages.. Each stage in the proposed design is resonant at different frequency to increase bandwidth. The three stages of the proposed LNA are as follow, first stage which is the input stage is common gate (CG) amplifier which introduced to provide high input impedance matching with the aid of inductor Ls which chosen to provide better impedance

matching. The second stage is cascode stage of two common source amplifier (CS) to increase gain and bandwidth performance. Also, this cascode stage will help in reduction of power dissipated for LNA. The third stage consists of Common Drain (CD) amplifier (M3) and diode connected transistor (M6), the Common Drain amplifier (CD) is used to drive high capacitive load of next stage and act as a buffer stage for output measurements. Diode connected load transistor is used to reduce output noise of LNA as follow, by replacing diode conected transistor with its equivalent resistance ($1/g_{m6}$) which is very small resistance and the effect of this as follow: when the transistor has its output impedance as a load, then the output noise of the transistor will be maximum. If the transconductance of MOS transistor is decreased, then as aresult its noise current will be reduced. So to achieve minimum output noise for the transistor it must have small transconductance, and minimum transconductance of the output transistor in the proposed LNA is achieved by connecting diode connected transistor in parallel with the output transistor (M4). As the equivalent resistance of diode connected transistor is very small ($1/g_{m6}$), so when it connected in parallel with the equivalent resistance of output transistor (M4) in LNA circuit, this will produce very small output transconductance for the amplifier and output noise of (M4) will be reduced and then the total output noise of proposed LNA will be reduced.

TABLE I summarizes the components value of the proposed LNA design.

IV. Proposed Ultra-Wideband Low Noise Amplifier Simulation Results

This section will introduce the simulation results of the proposed LNA and the discussion of these results also will be introduced. The simulation results includes Noise Figure (NF) analysis, third order input referred intercept point (IIP3), input and output return loss analysis (S_{11}, S_{22}), bandwidth, gain and noise performance of proposed LNA.

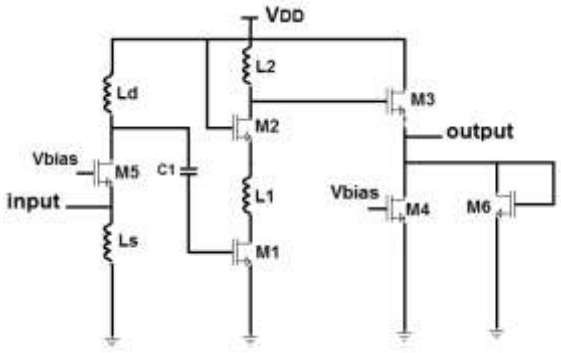

Fig. 4. Circuitry diagram of proposed UWB low noise amplifier

TABLE I. Summary of components value of proposed LNA

components	value	components	value
W1	5X40 um	Ls	1.6 nH
W2	5x40 um	Ld	0.5 nH
W3	1x25 um	C1	1.5 pF
W4	1x20 um	L1	1 nH
W5	5x40 um	L2	2.5 nH
W6	1x20 um	Vbias	0.3 V

TABLE II. Performance comparison for proposed and traditional LNA

Parameter	Traditional LNA	Proposed LNA
Technology	130 nm CMOS technology	130 nm CMOS technology
Power supply	3.2 V	1.2 V
Bandwidth	6.57 GHz	3.9-15 GHz
Gain	5 dB	10 dB
Output noise	2.26 mV_{rms}	300 uV_{rms}
Dissipated power	15.04 mW	1.2 mW
Noise figure (NF)	7 dB	1.5 dB

Also performance comparison will be made between traditional and proposed LNA. This comparison is introduced in TABLE II, as shown from the obtained results that the proposed LNA technique has better performance parameters than traditional one. The proposed LNA has small output noise value of 300 uV_{rms} because of using diode connected transistor at the output stage and as a result noise figure (NF) is reduced to 1.5 dB. The proposed LNA has high bandwidth from (3.9 GHz to 15 GHz) because of the reduction in the coupling capacitor C1 values and the elimination of C2 and some inductors that exist in traditional one. The proposed LNA has 1 mA total current using 1.2 V power supply, so proposed LNA has low dissipated power of 1.2 mW compared with traditional one which has dissipated power of 15.04 mW. From this comparison and these results it is clear that the proposed LNA has better parameter performance than traditional one. This ensure that the better effect of proposed LNA technique.

A. Mathematical Model for Noise Analysis of Proposed UWB LNA

The reduction in the output noise for the proposed UWB LNA due to adding diode connected transistor can be proved mathematically using a mathematical model. The first step in this mathematical analysis based on calculating the total output noise of the amplifier before and after adding diode connected transistor M6 at the output. Fig. 5 shows equivalent circuit for noise analysis before adding diode connected transistor and Fig. 6 shows small signal noise equivalent circuit before adding diode connected transistor. From these two figures we can calculate output noise components for the amplifier before adding M6 as follow: the output noise for the amplifier has two components, first noise component ($V_{n,out1}$) is due to transistors M3 and M4 as in (1) and (2).

$$V_{n,out1}(1 - g_{m3}Z_{out}) = (I_{n,M3} + I_{n,M4})Z_{ou} \quad (1)$$

Where: $V_{n,out1}$ is first noise component, g_{m3} is transconductance of transistor M3, $I_{n,M4}$ is noise current due to transistor M4, Z_{out} is output impedance of low noise amplifier, r_{ds3} is equivalent small signal impedance of transistor M3, r_{ds4} is equivalent small signal impedance of transistor M4, X_{CL} is load capacitive reactance.

$$Z_{out} = r_{ds3}//r_{ds4}//X_{CL} \quad (2)$$

The second component of output noise ($V_{n,out2}$) is due to equivalent resistance (R_n) of input transistor M5 and can be given using (3), (4) and (5).

$$V_{gs3} = V_{g3} - V_{s3} = I_{n,Rn}X_Z - V_{n,out2} \quad (3)$$

Where: V_{gs3} is small signal voltage of transistor M3, $I_{n,Rn}$ is noise current due to transistor M5, *Xz* is equivalent to $X_{Ld}//X_{C1}$, $V_{n,out2}$ is second noise component.

$$V_{n,out2} = g_{m3}V_{gs3}Z_{out} = g_{m3}Z_{out}(I_{n,Rn}X_Z - V_{n,out2}) \quad (4)$$

$$V_{n,out2}(1 + g_{m3}Z_{out}) = g_{m3}Z_{out}I_{n,Rn}X_Z \quad (5)$$

As shown from the previous equations and from the two components of output noise that the total output noise of the amplifier can be reduced by reducing the value of output impedance (Z_{out}) of the amplifier. The reduction in the output impedance of the amplifier can be occurred by adding the diode connected transistor M6 as shown in Fig. 7 and Fig. 8. As shown in Fig. 7, the equivalent circuit for noise analysis after adding diode connected transistor and Fig. 8 shows the small signal noise equivalent circuit after adding M6. By replacing diode connected transistor by its small signal equivalent which is very small resistance (r_{ds6}= $1/g_{m6}$) where, g_{m6} is transconductance of transistor M6. As this resistance (r_{ds6}) is very small resistance and connected in parallel with output resistance, so the total output resistance of amplifier will be reduced and then total output noise of the proposed amplifier will be reduced. This is the effect of adding diode connected transistor M6 on amplifier output noise reduction. This effect can be calculated mathematically as in the follow equations. For the first component of the noise ($V_{n,out1}$) which due to transistors (M3, M4 and M6) can be calculated using (6), (7) and (8).

$$V_{n,out1} = (I_{n,M3} + I_{n,M4} + I_{n,M6} + g_{m3}V_{n,out1})Z_{ou} \quad (6)$$

Where: $V_{n,out1}$ is first noise component, $I_{n,M3}$ is noise current due to transistor M3, $I_{n,M4}$ is noise current due to transistor M4, $I_{n,M6}$ is noise current due to transistor M6, g_{m3} is transconductance of transistor M3, Z_{out} is output impedance of amplifier.

$$Z_{out} = r_{ds3}//r_{ds4}//r_{ds6}//X_{CL} \quad (7)$$

Where: Z_{out} is the output impedance of the amplifier and in this case it is very small value due to equivalent small signal impedance of transistor M6 (r_{ds6}) is very small value, r_{ds3} is equivalent small signal impedance of transistor M3, r_{ds4} is equivalent small signal impedance of transistor M4, X_{CL} is load capacitive reactance.

$$V_{n,out1}(1 - g_{m3}Z_{out}) = (I_{n,M3} + I_{n,M4} + I_{n,M6})Z_{out} \quad (8)$$

The second component of noise is due to R_n and can be calculated using (9).

$$V_{n,out2}(1 + g_{m3}Z_{out}) = g_{m3}Z_{out}I_{n,Rn}X_Z \quad (9)$$

Where: X_Z is equivalent to $X_{Ld}//X_{C1}$.

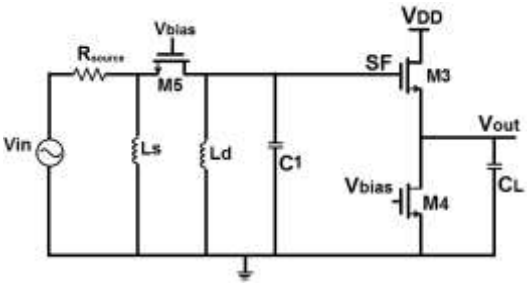

Fig. 5. Equivalent circuit for noise analysis before adding diode connected transistor M6

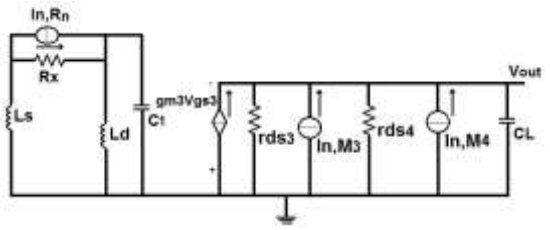

Fig. 6. Small signal model for noise analysis before adding M6

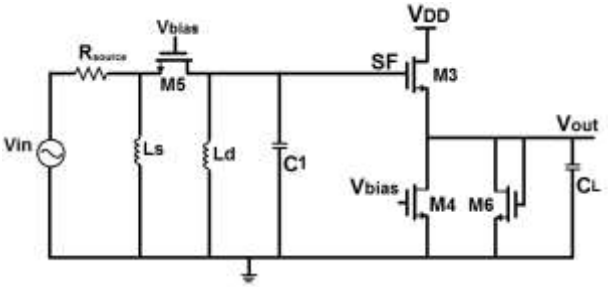

Fig. 7. Equivalent circuit for noise analysis after adding diode connected transistor M6

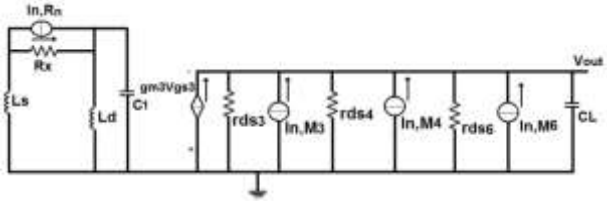

Fig. 8. Small signal model for noise analysis after adding M6

Finally to complete the noise analysis and to make sure that the proposed mathematical model is correct, we provided a comparison between the proposed simulated output noise results using cadence and using Matlab. This comparison is provided in Table 3, as shown in TABLE III that the two results are nearly equal, this proves that the proposed mathematical model is accurate. Fig. 9 shows the plotting of the output noise power spectral density for the amplifier before adding diode connected transistor M6 and Fig. 10 shows the plotting of output noise power spectral density for the amplifier after adding diode connected transistor. From these plots it is clear that the effect of adding diode connected transistor on the reduction of amplifier output noise.

TABLE III. Comparison between amplifier output noise before and after adding diode connected transistor M6 using cadence and Matlab

UWB LNA before adding M6	In cadence = 2.26 mv_{rms}	In Matlab = 3 mv_{rms}
UWB LNA after adding M6	In cadence = 300 uv_{rms}	In Matlab = 302 uv_{rms}

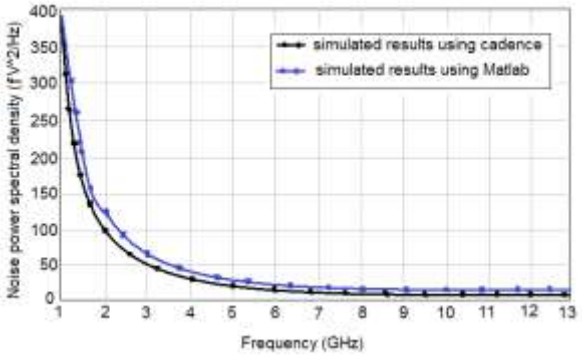

Fig. 9. Simulated output noise power spectral density of LNA before adding diode connected transistor M6 by cadence and Matlab

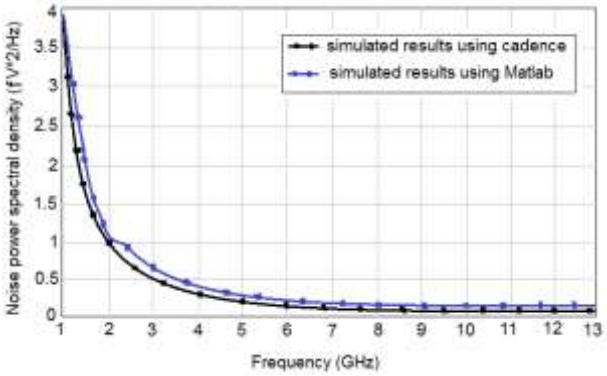

Fig. 10. Simulated output noise power spectral density of LNA after adding diode connected transistor M6 by cadence and Matlab

B. Proposed UWB Low Noise Amplifier Simulation Results

Noise figure analysis, noise figure represents noise performance of low noise amplifier. The simulation result of noise figure (NF) for the proposed UWB LNA is shown in Fig. 11. As shown the proposed LNA has low noise figure value of 1.5 dB, this reduction in noise figure value due to the reduction in the total output noise of LNA, which occurred by using diode connected transistor at the output stage.

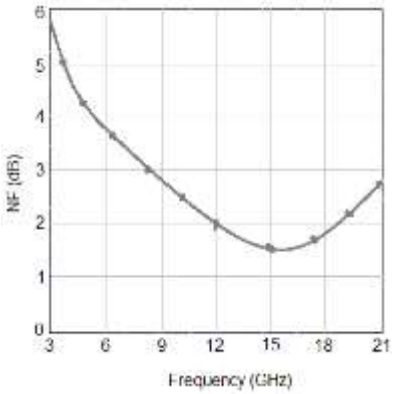

Fig. 11. Noise figure analysis simulation result

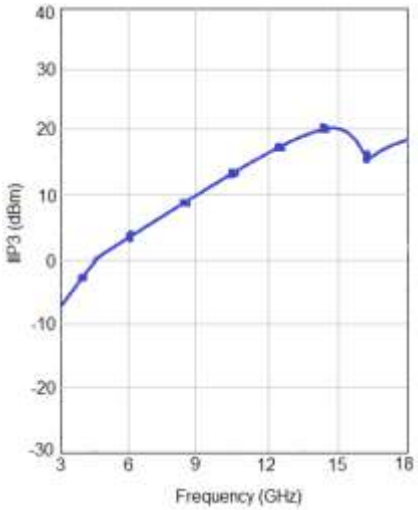

Fig. 12. IIP3 simulation results: IIP3 versus frequency of proposed LNA

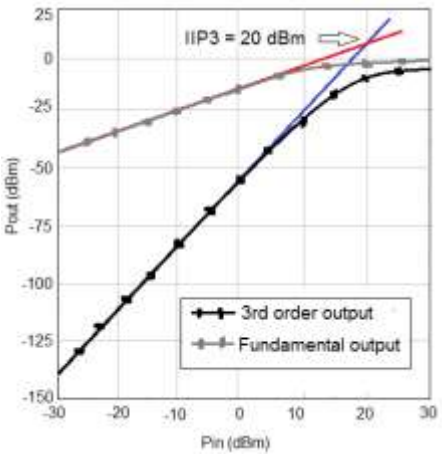

Fig. 13. IIP3 simulation results: input power versus output power of proposed LNA

Third order input referred intercept point (IIP3) analysis. IIP3 analysis measures the linearity of the system at specified frequency. In the proposed LNA design the IIP3 has been improved after adding diode connected transistor in parallel with output transistor of LNA, this technique introduces linearity to the amplifier so IIP3 parameter is improved. Simulation result of IIP3 is shown in Fig. 12 and Fig. 13. Fig. 12 represents relation between IIP3 with frequency. From the obtained results IIP3 reached to 20 dBm at operating frequency from 3.9 GHZ to 15 GHz. This result ensures that the proposed LNA has good linearity through the operating frequency range. Fig. 13 represents plot between input and output power of LNA amplifier, the plot ensure that the linearity of the proposed LNA has been improved as IIP3 reached to 20 dBm.

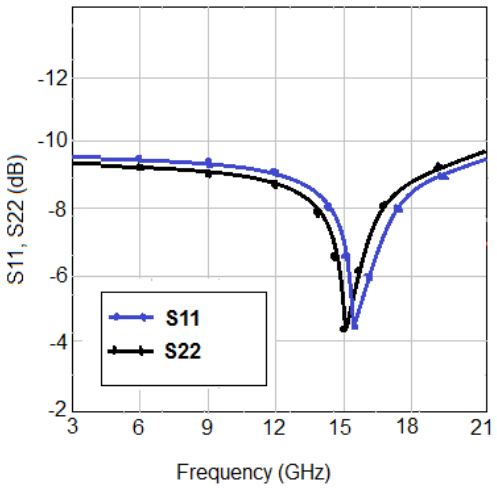

Fig. 14. S11 and S22 vs. frequency of proposed LNA

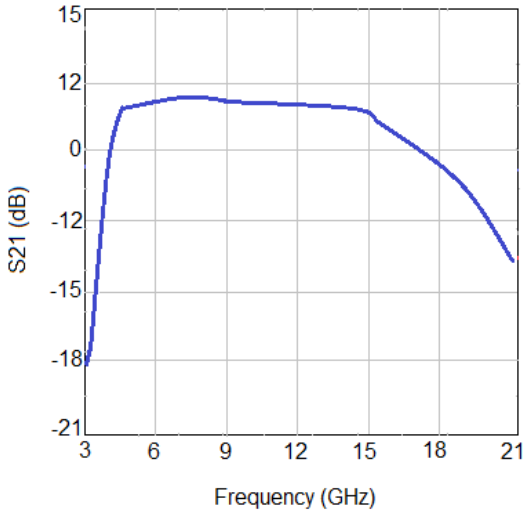

Fig. 15. Power gain of amplifier versus frequency

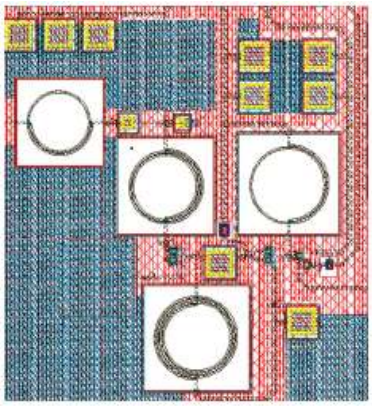

Fig. 16. Layout of the proposed UWB LNA

Input and output impedance matching coefficients (S11 and S22) and amplifier gain (S21). S11 and S22 coefficients measure impedance matching of amplifier. In the proposed LNA the impedance matching is improved by using common gate (CG) amplifier as input stage. Fig.14 shows simulation result for input and output impedance matching coefficient. As shown S11 value is less than -10 and S22 value is less than -10 this means that the proposed LNA has good impedance matching. The proposed amplifier provides power gain of 10 dB at frequency range from (3.9 GHz to 15 GHz) as shown in Fig. 15.

Layout of the proposed UWB LNA, The layout of the proposed UWB LNA is shown in Fig. 16. The proposed UWB LNA is implemented using 130 nm CMOS technology. Proposed LNA circuitry consists of 6 NMOS transistors, four inductors and one capacitor. The separating distance between amplifier components was kept to be small as possible to achieve small size design for proposed LNA.

TABLE IV. Post-layout simulation results

Parameter	Result
Technology	130 nm CMOS technology
Power supply (V_{DD})	1.2 V
Gain (S21)	10 dB
Bandwidth	15 GHz
Noise figure (NF)	1.5 dB
S11	-10 dB
IIP3	20 dBm
Dissipated power	1.2 mW
Output noise	300 uv_{rms}

Summary of the post layout simulation results, The post-layout simulation for the proposed UWB LNA is introduced in TABLE IV, as shown from the results, the proposed LNA provides wide bandwidth from 3.9 GHz to 15 GHz due to reducing coupling capacitor C1 value and removing coupling capacitor C2 and some inductors that existing in traditional one. The amplifier has low power consumption of 1.2 mW. The output noise of the proposed LNA is reduced to 300 uV_{rms} due to using diode connected transistor at the output stage and so the noise figure reached to 1.5 dB. LNA provides gain (S21) of 10 dB. Input and output impedance matching coefficient S11 is -10 dB and S22 is -10 dB. The input referred intercept point IIP3 is 20 dBm and total output noise is 300 uv_{rms}. These results make the proposed UWB LNA is suitable for ultra-wideband wireless application.

Performance comparison of the proposed UWB LNA and recently published LNA, Comparison between the proposed UWB LNA and the recently published LNA is introduced in TABLE V. All these comparison results and the proposed results are obtained by simulation. As shown from this comparison the proposed UWB LNA design having lowest power dissipation and lowest noise figure compared with others due to the proposed LNA technique. Finally, Proposed LNA have high bandwidth, high power gain, low power consumption, low output noise and low noise figure, so it is convenient for wireless communication applications.

TABLE V. Performance comparison of proposed LNA and recently published LNA

Reference	**This work**	[10]/2013	[11]/2015	[12]/2018	[13]/2019	[14]/2019	[15]/2021
Process	**130 nm CMOS Process**	180 nm CMOS Process	130 nm CMOS Process	180 nm CMOS Process	65 nm CMOS Process	65 nm CMOS Process	180 nm RF CMOS process
Power supply	**1.2 V**	---	---	1.8 V	1.2 V	1 V	1.2 V
Gain (S21)	**10 dB**	---	---	---	---	12.8 dB	10.8 dB
Bandwidth	**3.9-15 GHz**	2.5-16 GHz	2.35-9.37 GHz	3-12 GHz	3-10 GHz	55-64 GHz	3.1-10.6 GHz
Noise figure(NF)	**1.5 dB**	3.3 dB	3.68 dB	1.7-1.99 dB	2.8-3.1 dB	3.6 dB	2.5-4 dB
S11	**<-10 dB**	< -7 dB	< -8 dB	< -10 dB	< -8.7	-12 dB	-10 dB
IIP3	**20 dBm**	-5 dBm	- 4 dBm	-5.5 dBm	-5.7 dBm	-6 dBm	3.84 dBm
Dissipated power	**1.2 mW**	20 mW	9.97 mW	23.23 mW	18 mW	8.8 mW	6 mW

V. DISCUSSION

From the obtained simulation results it is clear that the proposed UWB LNA design technique has great performance compared with traditional one. From these results the noise figure of the proposed LNA is reduced to 1.5 dB and its linearity is increased compared with the traditional due to using diode connected load technique, as diode connected load technique gives nonlinearity in against direction of the nonlinearity which exist in the circuit and so the total nonlinearity of the circuit can be removed. In the proposed LNA the input referred third order intercept point (IIP3) reached to 20 dBm. The proposed LNA circuit dissipates low power reached to 1.2 mW compared with the traditional circuit which consumes 15.04 mW. The proposed LNA has wide bandwidth range from 3.9 GHz to 15 GHz.

VI. CONCLUSION

The proposed UWB LNA uses three stages amplifier with diode connected transistor. The proposed LNA is suitable for ultra-wideband wireless applications. The amplifier circuit is designed and implemented using 130 nm CMOS technology. Design parameters that obtained show that the proposed LNA has high bandwidth, low power consumption, low noise figure, high power gain and high linearity. The proposed LNA design technique improved a lot in the operation of UWB LNA and so will improve the performance of the whole UWB system.

REFERENCES

[1] X. Tong, S. Zhang, P. Zheng, Y. Huang, J. Xu, X. Shi, and R. Wang, "A 22-30-GHz GaN low-noise amplifier with 0.4-1.1-dB noise figure," IEEE Microwave and Wireless Components Letters, vol. 29, no. 2, pp. 134-136, 2019.

[2] G. R. Aiello, and G. D. Rogerson, "Ultra-wideband wireless systems," IEEE Microwave Magazine, vol. 4, no. 2, pp. 36-47, 2003.

[3] R. Karmakar, S. Chattopadhyay, and S. Chakraborty, "An online learning approach for auto link-configuration in IEEE 802.11 ac wireless networks," Computer Networks, 181, 2020.

[4] Y-L. Wei, S. S. Hsu, and J-D. Jin, "A Low-power low-noise amplifier for K-band applications," IEEE Microwave and Wireless Components Letters, vol. 19, no. 2, pp. 116-118, 2009.

[5] C-C. Wu, M-F. Chou, W-S. Wuen, and K-A. Wen, "A low power CMOS low noise amplifier for ultra-widband wireless applications," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 5063-5066, 2005.

[6] J. Jung, T. Yun, J. Choi, and H. Kim, "Wideband and low noise CMOS amplifier for UWB recievers," Microwave and Optical Technology Letters, vol. 49, no. 4, pp, 749-752, 2007.

[7] J. Khalife, M. Neinavaie, and Z. M. Kassas, "Universal receiver architecture for blind navigation with partially known terrestrial signals of opportunity," Processing of the 34th International Technical Meeting of the Satellite Division of The Institute of Navigation (ION GNSS+ 2021), pp. 2201-2211, 2021.

[8] T. Kojima, H. Kiuchi, K. Uemizu, Y. Uzawa, M. Kroug, A. Gonzalez, T. Dippon, and T. Kageura, "Demonstration of a wideband submillimeter-wave low-noise receiver with 4-21 GHz IF output digitized by a high-speed 32 GSps ADC," Astronomy & Astrophysics, 640, 2020.

[9] S. Rozowicz, and A. Zawadzki, "Experimental verification of signal propagation in automotive ignition cables modelled with distributed parameter circuit," Archives of Electrical Engineering, vol. 68, no. 3, 2019.

[10] K. Yousef, H. Jia, R. Pokharel, A. Allam, M. Ragab, H. Kanaya, and K. Yoshida, "CMOS ultra-wideband low noise amplifier design," International Journal of Microwave Science and Technology, pp. 40-45, 2013.

[11] S. Arshad, R. Ramzan, K. Muhammad, and Q-U. Wahab, "A sub-10mW, noise canceling, wideband LNA for UWB applications," International Journal of Electronics and Communications (AEU) Elsevier, vol. 69, no. 1, pp. 109-118, 2015.

[12] M. Hayati, S. Cheraghaliei, and S. Zarghami, "Design of UWB low noise amplifier using noise-canceling and current-reused techniques," Integration 60, pp. 232-239, 2018.

[13] L. Luo, M. Liu, L. Chen, J. Gao , Z. Zhu, and Y. Yang, "A 2.99 dB NF 15.6 dB gain 3-10 GHz ultra-wideband low-noise amplifier for UWB system in 65 nm CMOS," Analog Integrated Circuits and Signal Processin, vol. 101, no. 3, pp. 651-657, 2019.

[14] M. Yaghoobi, M. Yavari, M. H. Kashani, H. Ghafoorifard, and S. Mirabbasi, "A 55-64-GHz low-power small-area LNA in 65-nm CMOS with 3.8-dB average NF and ~ 12.8-dB power gain," IEEE Microwave and Wireless Components Letters, vol. 29, no. 2, pp. 128-130, 2019.

[15] B. D. Yaghouti, and J. Yavandhasani, "A high linearity low power low-noise amplifier designed for ultra-wide-band receivers," Analog Integrated Circuits and Signal Processing, vol. 107, no. 1, pp. 109-120, 2021.